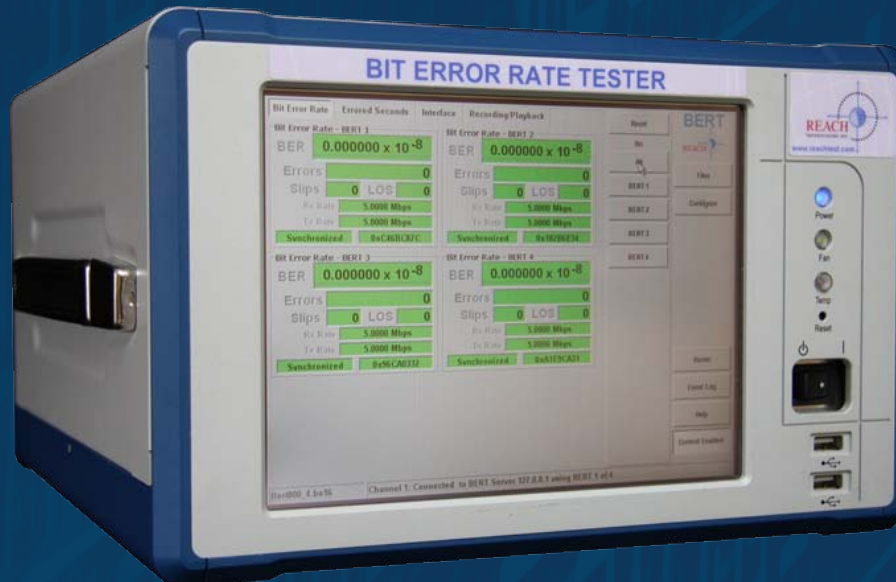


BIT ERROR RATE TESTERS

BERT

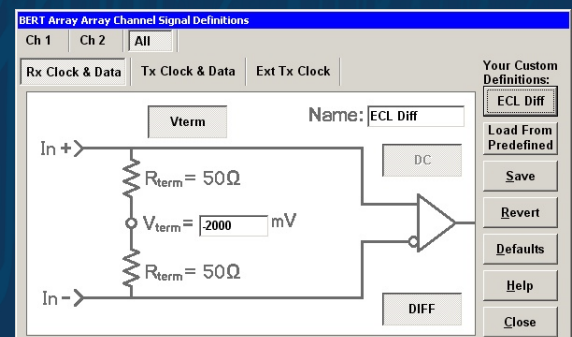
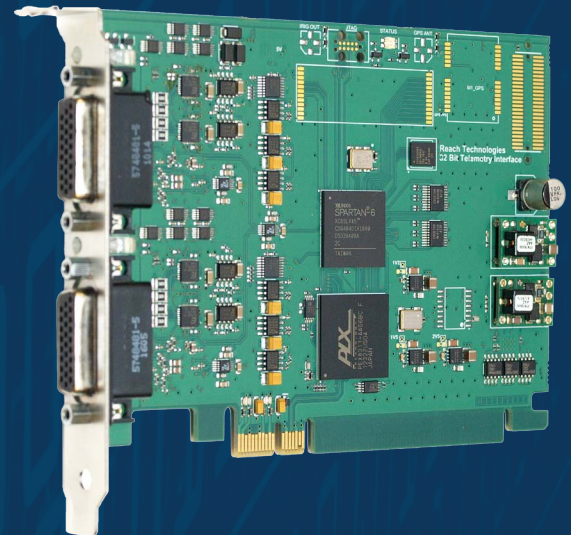
Sets the standard in BER testing for serial data links

Reach Technologies Inc. BER Testers are designed for testing serial communications equipment, communications links and radio telemetry systems. In addition to several standard configurations, Reach also offers custom configurations, including multi-channel and mixed data rates.



Features

- Flexible Configurations
 - ◊ High-speed - 1 Gbps to 58 Gbps
 - ◊ Mid-speed - 100 Mbps to 1 Gbps
 - ◊ Low-speed - 100 bps to 100 Mbps
 - ◊ Several stand-alone chassis options
 - ◊ PC-board & embedded module options
 - ◊ External TX clock input
- Multi-Channel
 - ◊ Up to 14 channels per chassis
- High Data Rates
 - ◊ Supports "gapped" or "burst" clocking
- High-Speed I/O
 - ◊ Supports LVDS, ECL, and customer specific
- Mid & Low-Speed I/O
 - ◊ Programmable I/O electrical levels
 - ◊ Supports TTL, RS-422, LVDS, ECL, PECL, etc.
- Remote Control
- Latency Measurement
 - ◊ Measures end-to-end and round trip delay
- I/Q Testing
 - ◊ Common TX & RX clocks for QPSK testing
- Statistic Recording
 - ◊ User-defined trigger thresholds
 - ◊ Playback BER stats for detailed investigations
- Optional Statistical Eye Diagram
- Optional Noise Injection
- Optional Jitter Injection



BIT ERROR RATE TESTERS

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Sets the standard in BER testing for telemetry systems

Technical Specifications

Checker

- Input data from min to max rate
- 1×10^{-2} maximum BER detected
- 2×10^{-16} minimum BER detected
- Errored seconds statistics
- Display of actual received data rate
- Data decode
 - ◊ RNRZ-L, NRZ-L, NRZ-M, NRZ-S
 - ◊ async NRZ and bi-phase
- PRBS patterns
 - ◊ $2^{23}-1$, $2^{15}-1$, $2^{11}-1$ and 2^7-1
 - ◊ 8 to 2040 bits of zero in PRBS patterns
 - ◊ 3-bit to 32-bit patterns
 - ◊ 8 user-defined patterns

Generator

- Internal clock synthesizer
 - ◊ min to max rate
- External clock input
- Display of actual transmitted data rate
- Data encode
 - ◊ RNRZ-L, NRZ-L, NRZ-M, NRZ-S
 - ◊ async NRZ and bi-phase
- PRBS patterns
 - ◊ $2^{23}-1$, $2^{15}-1$, $2^{11}-1$ and 2^7-1
 - ◊ 8 to 2040 bits of zero in PRBS patterns
 - ◊ 3-bit to 32-bit patterns
 - ◊ 8 user-defined patterns
- Bit error insertion
 - ◊ single button push
 - ◊ periodic

User Interface

Reach Technologies Inc. BER Testers have an intuitive GUI that displays statistics and allows complete user control over the system - both locally and remotely.

Control

- Input
 - ◊ Data polarity
 - ◊ Clocking edges
 - ◊ Data decoding
 - ◊ PRBS or user pattern
- Output
 - ◊ Bit rate
 - ◊ Data polarity
 - ◊ Clock edges
 - ◊ Data encoding
 - ◊ PRBS or user pattern
 - ◊ Error insertion

Displays

- 1 to ∞ sec BER calc interval
- Bit error rate
- Bit errors & slips
- Actual RX clock rate
- Actual TX clock rate
- Statistics
 - ◊ Errored seconds
 - ◊ Bit slip seconds
 - ◊ Sync loss seconds
 - ◊ RX data loss seconds
 - ◊ RX clock loss seconds



Ordering Options

BERT-XXXXX-##-FFFF

XXXXX

FFFF

Maximum Data Rate
Number of Channels
Form Factor

{ 100M: 100 Mbps, 1G: 1 Gbps, 6G: 6.6 Gbps, 12G: 12.5 Gbps, 28G: 28 Gbps, 58G: 58 Gbps }
{ Chassis dependent }
{ B: Benchtop, P: Portable, R: 19" Rack, W: Workstation, PCIE: PCIe Card, E: Embedded Module }

Additional Options

TM-IO-XXX
CBL-TM-IO-XXX
BERT-SDK
BERT-CBX
BERT-EYE
BERT-NOISE
BERT-JITTER

I/O Interface Module
I/O Cable
Software Development Kit
Crossbar Switch
Eye Diagram
Noise Injection
Jitter Injection

{ SMA, TRIAX, BNC }
{ SMA, TRIAX, BNC }